Scalable Modeling with Simple Topology for Stacked Millimeter-Wave Transformers

Diqun Lu, Wenjuan Zhang, and Fujiang Lin

Department of Electronic Science and technology
University of Science and Technology of China (USTC), Hefei, China 230027
Email: linfj@ustc.edu.cn

Abstract — **Scalable modeling with very simple topology for stacked millimeter-wave transformers is presented. The simplified model is based on single-π and double-π network for transformers with turn ratio 1:1 and 1:2, respectively. Compared with the previous models, the architecture is much simpler while maintaining good model performance. A very close agreement is shown for S-parameter, self-inductances of each coil and coupling coefficient up to 110GHz.**

Index Terms **—Transformers modeling, Scalable equivalent circuit, Electromagnetic simulation.**

I. Introduction

Recently, interest in on-chip transformer has surged for the capability of impedance conversion and low loss while occupying reduced silicon area. Transformers have been used as inter-stage connection in the power amplifier of [1], as low-loss devices in the ASK modulator of [2], and as feedback elements in the low-noise amplifier of [3].

Because of the wide application of transformers in millimeter-wave (mm-wave) silicon-based circuits, modeling for transformers has become more and more essential. Two effective approaches are proposed to model the behavior of transformers. Models extracted from the EM simulation can be time-consuming and complicated to provide a reliable result. Hence, equivalent circuits based on geometric and process data developed. However, EM simulation tested by measurement can offer an alternative way to verify the scalable models.

A model based on fabrication specifications is presented in [4], which is verified by comparison with experimental measurements of interleaved transformers up to 10GHz. *B.Leite et al.* [5] present an analytical model for stacked transformers, which shows a close agreement with measured values up to 110GHz. Likewise, In [6] and [7], scalable models with complicated parasitic equivalent circuits and alternative model architectures are introduced, respectively. However, architectures or equations of analytical models now available are complicated.

In this paper, a scalable model with very simple topology for stacked transformers is introduced. The simplified model is based on single-π and double-π network for transformers with turn ratio 1:1 and 1:2, respectively. The very simple topology is presented in section II. EM simulation is tested in section III-A and the simplified model is verified and compared with the original model in section III-B. Conclusions are drawn in section IV.

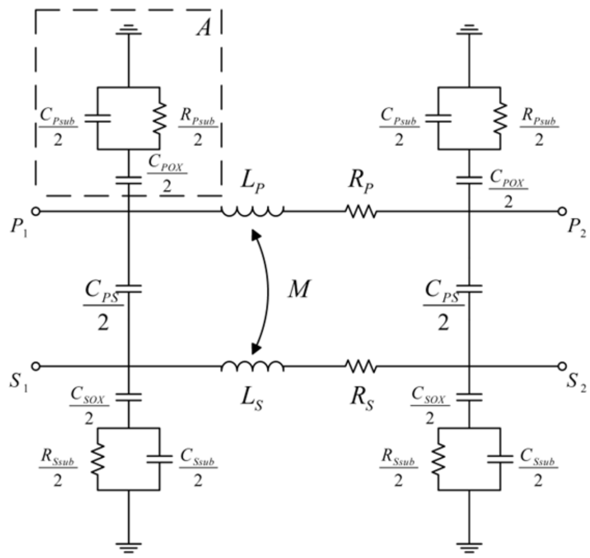

Fig. 1. Simplified model for transformers with turn ratio 1:1.

II. Simplified Model

Maintaining enough accuracy, a perfect model must be simple both in the topology and equations at the same time.

Fig 1 shows the simplified model architecture for stacked transformers with turn ratio 1:1. In the circuit, the primary coil and secondary coil are modeled by modified single-π network [8], where L_p and L_s represent inductance of each coil, respectively. The resistors R_p and R_s are frequency dependent, which takes into consideration the influence of the skin effect. The four shunt models (denoted as A in Fig 1) account for the capacitive coupling between the metal layer and substrate of each port, respectively. The electric and magnetic interaction between individual coils is modeled by the mutual inductance and capacitance C_{ps} .

The simplified model in Fig 2 based on double-π network is proposed because the architecture in Fig 1 is not accurate enough for stacked transformers with turn ratio 1:2. The secondary winding consists of two coils and each coil is modeled by series component (denoted as B in Fig 2).

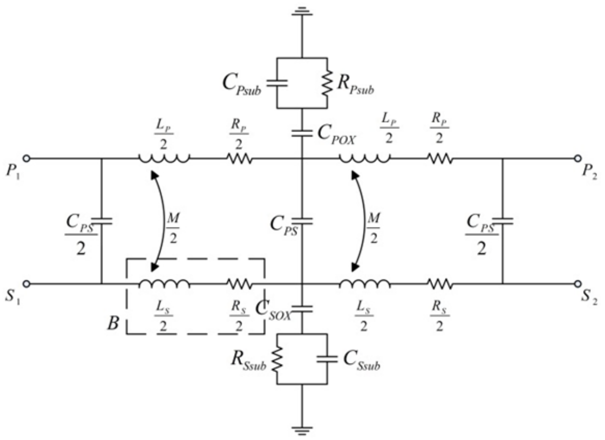

Fig. 2. Simplified model for transformers with turn ratio 1:2.

Similarly, the primary winding can be divided into two parts. The electric and magnetic interaction of each part is considered, respectively. And the capacitive coupling between each metal layer and substrate is modeled together.

Values of components in the model can be obtained by very simple calculation in [5], so the calculation is also used in this paper.

III. MODEL VERIFICATION

The transformer with a 116-μm diameter and a 4-μm trance wide was fabricated in 65-nm CMOS from SMIC. The on-chip transformer has been de-embedded by open-short method [9] and S-parameter was measured using the Agilent PNA E8364C network analyzer covering frequencies up to 50GHz. Fig 3 shows the micrograph of the transformer and open-short test structure.

A. *EM simulation*

EM simulations were carried out to verify the model. The dielectric layers are replaced by three equivalent layers, one between primary and air, one between primary and secondary, and the other between secondary and substrate. The dielectrics were simplified by the equation in [10].

$$\varepsilon_{req} = \left[\sqrt{\varepsilon_n} + \frac{h_{n-1}}{h_{n-1}+h_n}\left(\sqrt{\varepsilon_{n-1}} - \sqrt{\varepsilon_n}\right) \right]^2 \qquad (1)$$

Two ports were connected to ground and all the information of the transformer can be extracted from the other employed two-port characterization.

In order to validate that the EM simulation setup is reliable, the results of measurement and EM simulation from ADS Momentum electromagnetic field solvers are compared in Fig 4, which shows a good agreement.

B. *Model verification*

The simplified model has been verified by the EM simulation of SMIC 65nm CMOS transformers. The verification was effectuated through S-parameter, self-inductances of each coil as well as coupling coefficients.

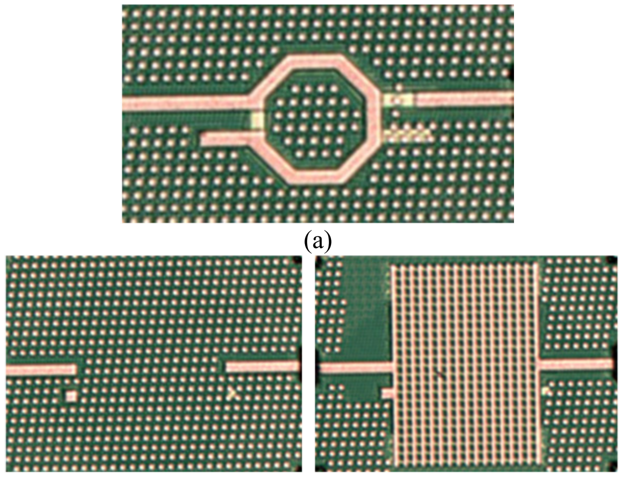

Fig. 3. The die photograph of (a) the transformer (b) open test structure and (c) short test structure.

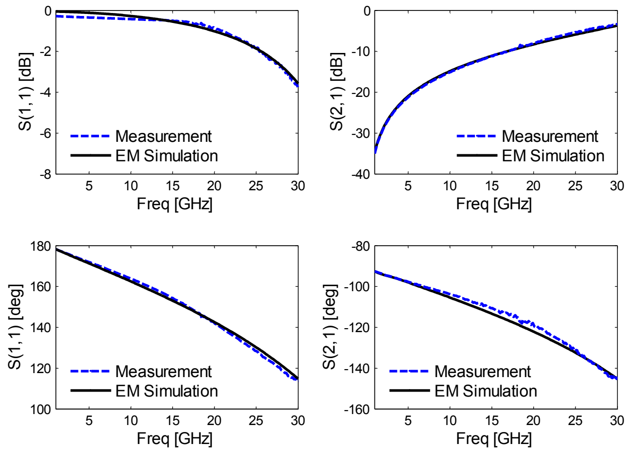

Fig. 4. Comparison of results from measurement and EM simulation from ADS Momentum electromagnetic field solvers.

TABLE I TRANSFORMRS TOPOLOGY

<table>
<tr><th rowspan="2"></th><th colspan="2">Primary</th><th colspan="3">Secondary</th><th rowspan="2">Process (nm)</th></tr>
<tr><th>Diameter (μm)</th><th>Width (μm)</th><th colspan="2">Diameter (μm)</th><th>Width (μm)</th></tr>
<tr><td>T1</td><td>60</td><td>12</td><td colspan="2">60</td><td>12</td><td>65</td></tr>
<tr><td>T2</td><td>60</td><td>4</td><td>60</td><td>48</td><td>4</td><td>65</td></tr>
</table>

Transformers with different structures in Table I have been simulated and modeled. Simulations were carried out from dc to 110GHz and Figs. 5-6 compare the results of EM simulation (ADS Momentum) to the simplified model, which shows a good agreement.

Compared with the previous model in [5], it is obvious that the original and simplified models show a close agreement with the results of EM simulation from Fig. 7. Therefore, the simplified model is simpler than the previous one and maintains enough accuracy at the same time.

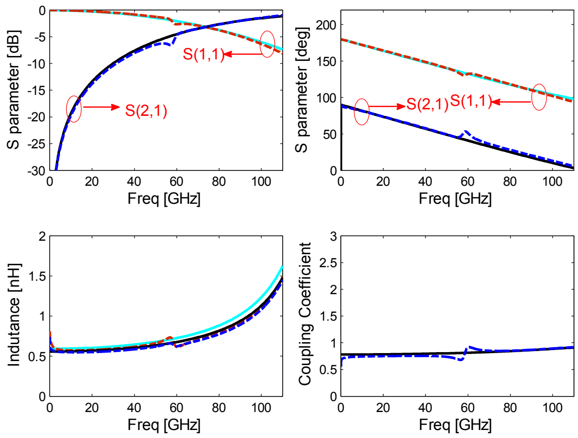

Fig. 5. Comparison between model (black or light blue solid line) and simulation (blue or red dotted line) for T1 in Table I.

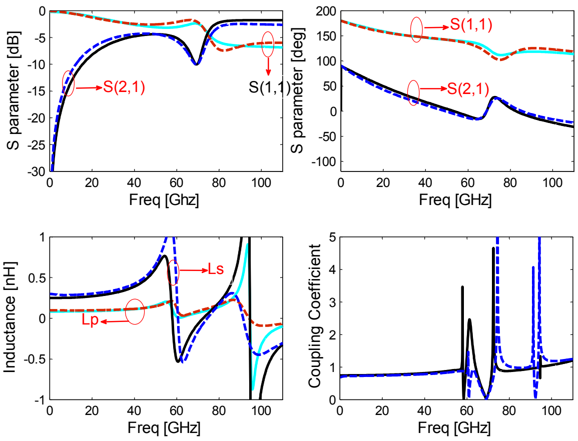

Fig. 6. Comparison between model (black or light blue solid line) and simulation (blue or red dotted line) for T2 in Table I.

IV. Conclusion

Transformers play a major role on the performance of present silicon-based integrated circuits and modeling for transformers is of special importance. A simplified model for stacked millimeter-wave transformers is proposed. A very close agreement up to 110GHz was shown for S-parameter, self-inductances of each coil and coupling coefficient. The simplified model is based on simpler architecture, which makes model for transformers convenient.

Acknowledgment

The authors would like to thank Information Science Laboratory Center of USTC for the software & hardware services. They would also like to acknowledge MediaTek for USTC students and project sponsorship.

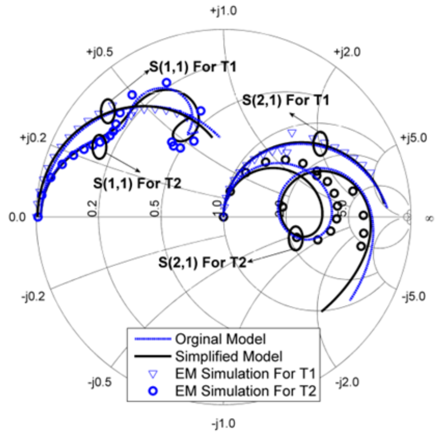

Fig. 7. Comparison between original model in [5] and simplified model for T1and T2 in Table I.

References

[1] D. B. Hou, W. Hong, W. L. Goh, Y. Z. Xiong, M. A. Arasu, J. He, J. X. Chen, and M. Madihian, "Distributed Modeling of Six-Port Transformer for Millimeter-Wave SiGe BiCMOS Circuits Design," *IEEE Trans. Microw. Theory Tech.,* vol. 60, no. 12, pp. 3728-38, Dec. 2012.

[2] J. Brinkhoff, D.-D. Pham, K. Kang, and F. Lin, "A New Six-Port Transformer Modeling Methodology Applied to 10-dBm 60-GHz CMOS ASK Modulator Designs," *IEEE Trans. Microw. Theory Tech.,* vol. 58, no. 2, pp. 297-309, Feb. 2010.

[3] C.-T. Fu, C.-N. Kuo, and S. S. Taylor, "Low-Noise Amplifier Design With Dual Reactive Feedback for Broadband Simultaneous Noise and Impedance Matching," *IEEE Trans. Microw. Theory Tech.,* vol. 58, no. 4, pp. 795-806, Apr. 2010.

[4] C. Wang, H. Liao , Y. Xiong, C. Li, R. Huang, and Y. Wang, "A Physics-Based Equivalent-Circuit Model for On-Chip Symmetric Transformers With Accurate Substrate Modeling," *IEEE Trans. Microw. Theory Tech.,* vol. 57, no. 4, pp. 980-90, Apr. 2009.

[5] B. Leite, E. Kerherve, J. B. Begueret, and D. Belot, "An Analytical Broadband Model for Millimeter-Wave Transformers in Silicon Technologies," *IEEE Trans. Electron Devices.,* vol. 59, no. 3, pp. 582-9, May. 2012.

[6] L. F. Tiemeijer, R. M. T. Pijper, C. Andrei, and E. Grenados, "Analysis, Design, Modeling, and Characterization of Low-Loss Scalable On-Chip Transformers," *IEEE Trans. Microw. Theory Tech.,* vol. 61, no. 7, pp. 2545-57, Jul. 2013.

[7] W. Zhang, G. Zhu, L. Sun, and F. Lin, "Scalable Modeling of layout parameters in CMOS integrated stacked millimeter wave Transformer," in *IEEE MTT-S International Wireless Symposium (IWS),* 2014.

[8] G. Zhu, W. Zhang, L. Sun, and F. Lin, "Analytical interconnect modeling based on equivalent circuit method," in *IEEE Electronics Packaging Technology Conference (EPT),* 2013, pp. 240-3.

[9] B. Leite, E. Kerherve, J. B. Begueret, and D. Belot, " Design and Characterization of CMOS Millimeter-Wave Transformers," in *IEEE MTT-S International Microwave & Optoelectronics Conference (IMOC),* 2009, pp. 402-6.

[10] A. Siligaris, C. Mounet, B. Reig, and P. Vincent, "CPW and discontinuities modeling for ircuit design up to 110 GHz in SOI CMOS technology," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium,* 2007, pp. 295-298.